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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,461	03/07/2002	Masataka Ito	00862.022541	8794

5514 7590 06/13/2002

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EXAMINER

ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 06/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/091,461

Applicant(s)

ITO, MASATAKA

Examiner

Stanetta D. Isaac

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 10-17 is/are pending in the application.
- 4a) Of the above claim(s) 9 and 18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10-17 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 5) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

Art Unit: 2812

DETAILED ACTION

Election/Restrictions

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Karl Quinn on 06/07/02 with traverse, in addition, the attorney did not give any reason for traverse.

Claims 9 and 18 are cancelled.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-8 and 10-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Sato et al. Patent Number 6180497.

Sato discloses:

(Col. 2 lines 61-67; col. 3 lines 7-9, 50-62; col. 7 lines 67 continued to col. 8 lines 1; col.

8 lines 30-37, 39-43)

Art Unit: 2812

1. An annealing method of annealing an SOI substrate

(Col. 2 lines 1-6, 61-67; col. 3 lines 7-9, 50-62; col. 7 lines 67 continued to col. 8 lines 1;
col. 8 lines 30-37, 39-43)

in a reducing atmosphere, comprising the step of:

holding the SOI substrate by a holding portion

having a surface formed from silicon and annealing the

SOI substrate.

2. The method according to claim 1, wherein the
annealing is executed at a temperature lower than a
melting point of single-crystal silicon.

(col. 7 lines 67 continued to col. 8 line 1)

3. The method according to claim 1, wherein the
annealing is executed at a temperature not less than
775°C.

4. The method according to claim 1, wherein the
annealing is executed at a temperature not less than
966°C.

5. The method according to claim 1, wherein the
annealing is executed at a temperature not less than
993°C.

6. An SOI substrate manufactured using an annealing

method of any one of claims 1.

(col. 3 lines 7-9, 50-62)

7. The substrate according to claim 6, wherein an HF defect density is not more than 0.05 defects /CM².

(col. 8 lines 30-37, 39-43)

8. A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of any one of claims 1; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

(Col. 2 lines 1-6, 61-67; col. 3 lines 7-9, 50-62; col. 7 lines 67 continued to col. 8 lines 1; col. 8 lines 30-37, 39-43)

10. An annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the SOI substrate by a holding portion which contains no silicon carbide formed by sintering and has a surface formed from silicon carbide deposited by CVD and annealing the SOI substrate.

11. The method according to claim 10, wherein the

annealing is executed at a temperature lower than a melting point of single-crystal silicon.

12. The method according to claim 10, wherein the annealing is executed at a temperature not less than 775°C.

13. The method according to claim 10, wherein the annealing is executed at a temperature-not less than 966°C.

14. The method according to claim 10, wherein the annealing is executed at a temperature not less than 993°C.

15. An SOI substrate manufactured using an annealing method of any one of claims 10.

16. The substrate according to claim 15, wherein an HF defect density is not more than 0.05 defects/cm².

17. A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of any one of claims 10; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

Art Unit: 2812

(Col. 2 lines 1-6, 61-67; col. 3 lines 7-9, 50-62; col. 7 lines 67 continued to col. 8 lines 1; col. 8 lines 30-37, 39-43)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
June 11, 2002


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800